

FIG. 1a

100 MEMORY DATA-A DATA-B -110 118 -[11 160a </bob 11 -16la 161b 107 117 120 MULTIPLIER ALU 412 140 ACCUMULATOR. 180 115 176 LOGIC FOR -150 WORD CONDITIONING

AND/OR ANALYSIS OPERATIONS

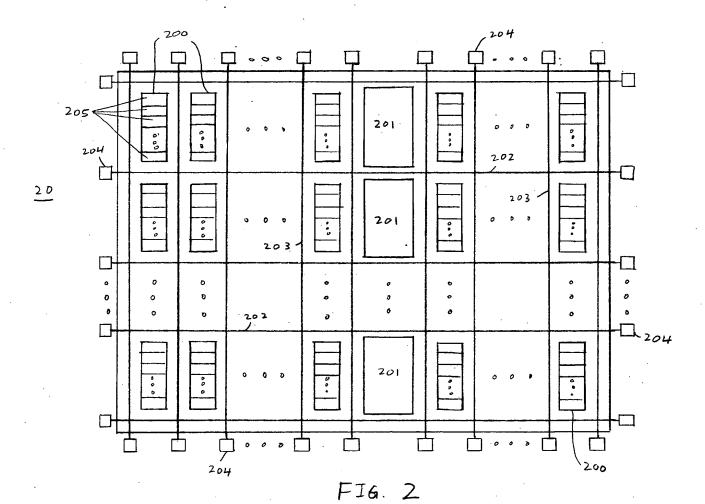
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Applicant: Martin Langhammer Sheet 3
Atty. Docket: 174/205
Title: DSP PROCESSOR ARCHITECTURE
WITH WRITE DATAPATH WORD
CONDITIONING AND ANALYSIS



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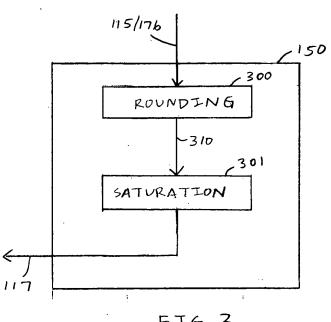


FIG. 3

Applicant: Martin Langhammer Sheet 4
Atty. Docket: 174/205
Title: DSP PROCESSOR ARCHITECTURE
WITH WRITE DATAPATH WORD
CONDITIONING AND ANALYSIS Sheet 4 of 8 450 4SIP "100...001" FROM ROUNDING LOGIC 4519 310 470 301 504 407 417 414 ± 7 400 MSB FROM ACCUMULATOR, ALU, ETC. MSB FROM ROUNDING LOGILC ナギ

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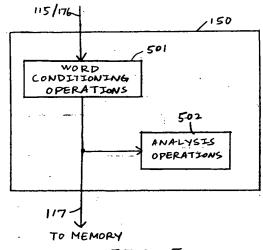
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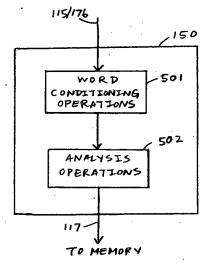
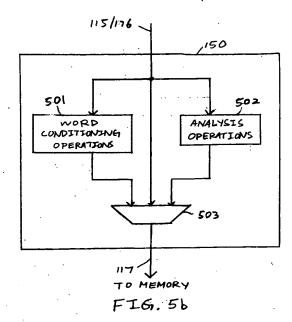
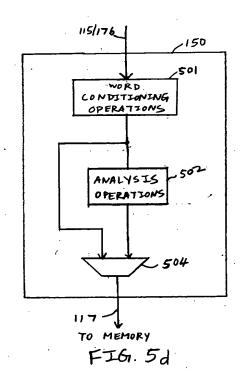


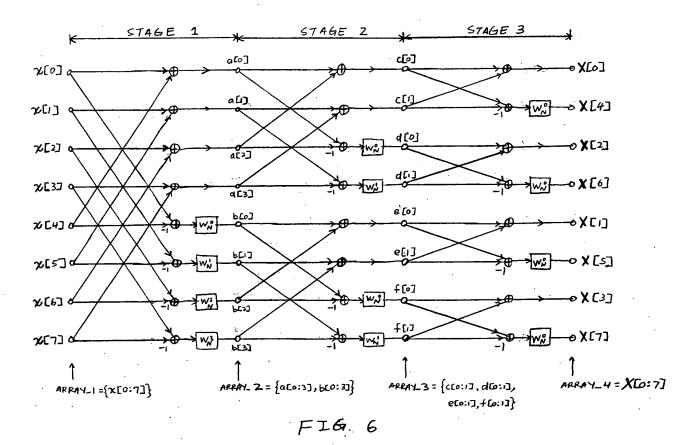
FIG. 5c





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WITH WRITE DATAPATH WORD
CONDITIONING AND ANALYSIS



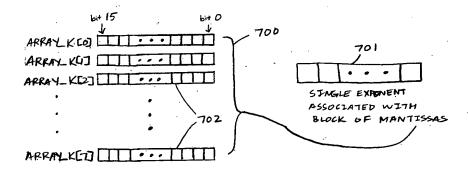


FIG. 7

ARRAY_Kour[p] or ARRAY_Kour[g]

FIG. 8

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BLOCK FLOATING

POINT CHECK

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